What is claimed is:

1. The semiconductor memory device, comprising:

a first cell array including a plurality of unit cells to be selected by an address signal;

a sense amplifying unit for sensing and amplifying voltage level of a bit line connected to the plurality of the unit cells;

a switching unit for connecting or disconnecting the sense amplifying unit to the bit line; and

a sense amplifying connection unit for controlling the switching unit for connecting or disconnecting the sense amplifying unit to the first cell array by increasing or decreasing an amount of current throughout the switching unit in response to the address signal.

2. The semiconductor memory device as recited in claim 1, wherein the sense amplifying connection unit includes:

a first sense amplifying connect control block for controlling a first amount of the current throughout the switching unit, when the first cell array is selected;

a sense amplifying disconnect control block for turning the switching unit off since voltage level of the unit cell is supplied to the bit line until the sense amplifying unit amplifies voltage level of the bit line;

a second sense amplifying connect control block for controlling a second current capability, which is less than

the first amount of amount of the current, throughout the switching unit when the first cell array is not selected; and

a sense amplifying reconnect control block for controlling the second sense amplifying connect block for flowing the second amount of the current throughout the switching unit; and controlling the first amount of the sense amplifying connect block for flowing the first amount of the current throughout the switching unit, after the sense amplifying unit finishes to amplify voltage level of the bit line.

3. The semiconductor memory device as recited in claim 2, wherein the sense amplifying reconnect block includes:

a disconnect signal generating block for outputting a second disconnect signal having more long pulsing time than a first disconnect signal after receiving the first disconnect signal for transiently disconnecting the first cell array to the sense amplifying unit;

a first reconnect control block for disabling the first sense amplifying connect block for inputting the second disconnect signal; and

a second reconnect control block for enabling the second sense amplifying connect block for time gap between pulse sections of the first disconnect signal and the second disconnect signal.

4. The semiconductor memory device as recited in claim 3,

wherein the disconnect signal generating block includes:

a delay block for delay block for time gap between pulse sections of the first disconnect signal and the second disconnect signal; and

a first NOR gate for outputting the second disconnect signal after receiving the first disconnect signal at one terminal and a output of the delay block at the other terminal.

5. The semiconductor memory device as recited in claim 4, wherein the first reconnect control block includes:

a first inverter for inversing a signal selecting a second cell array included in the other side of the sense amplifying unit; and

a second NOR gate for outputting a signal disabling the first sense amplifying connect control block after receiving the second disconnect signal at one terminal and the first inverter at the other terminal.

6. The semiconductor memory device as recited in claim 5, wherein the second reconnect control block includes:

a second inverter for receiving, inversing, and outputting the second disconnect signal; and

a third NOR gate for outputting a signal enabling the second sense amplifying connect block after receiving the first disconnect signal at one terminal and output of the second inverter at the other terminal.

7. The semiconductor memory device as recited in claim 6, wherein the first sense amplifying connect control block includes:

a first NAND gate for receiving output of the second NOR gate at one terminal and a signal for selecting the first cell array at the other terminal; and

a first PMOS transistor for delivering a first voltage for flowing the first current capability in the switching unit to the switching unit after receiving output of the first NAND gate at gate.

8. The semiconductor memory device as recited in claim 7, wherein the first sense amplifying connect control block further includes a first level shifter for outputting to gate of the first PMOS transistor after shifting a signal outputted from the first NAND gate to the first voltage level.

9. The semiconductor memory device as recited in claim 7, wherein the second sense amplifying connect control block includes:

a forth NOR gate for receiving output of the third NOR gate at one terminal and a signal for selecting all the first and the second cell arrays included in both side of the sense amplifying unit at the other terminal; and

a PMOS transistor for delivering a second voltage for flowing the second current capability in the switching unit to the switching unit after receiving output of the forth NOR

gate at gate.

10. The semiconductor memory device as recited in claim 9, wherein the second sense amplifying connect control block further includes a second level shifter for outputting to gate of the second PMOS transistor after shifting a signal outputted from the forth NOR gate to the second voltage level.

11. The semiconductor memory device as recited in claim 7, wherein the sense amplifying disconnect control block includes:

a third inverter for inversing and outputting the first disconnect signal;

a second NAND gate for receiving a signal for selecting the second cell array included in the other side of the sense amplifying unit at one terminal and output of the third inverter at the other terminal; and

a NMOS transistor for delivering a third voltage for turning the switching unit off after receiving output of the second NAND gate at gate to the switching unit.

12. The semiconductor memory device as recited in claim 1, wherein the switching unit includes at least one MOS transistor.

13. A method for executing a semiconductor memory device having a cell array including a plurality of unit cells, a

sense amplifier for sensing and amplifying voltage level of a bit line connected to the plurality of the unit cells, and a switching transistor for connecting or disconnecting the sense amplifying unit to the bit line, comprising the steps of:

(a) connecting the cell array to the sense amplifier by turning the switching transistor off;

(b) supplying voltage level of a data signal stored in the unit cell of the cell array;

(c) disconnecting the bit line to the sense amplifier by turning the switching transistor off;

(d) sensing and amplifying voltage appearing on the bit line by the sense amplifier unit;

(e) E providing the a first current to the switching transistor by supplying a first voltage to gate of the switching transistor; and

(f) reconnecting the cell array to the sense amplifying unit by providing a second current throughout the switching transistor after supplying a second voltage being higher than the first voltage to gate of the switching transistor.

14. The method for executing a semiconductor memory device as recited in claim 13, further comprising, before the step (a), the step of providing the first current throughout the switching transistor by supplying the first voltage to gate of the switching transistor.